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## Cortus announces Processor IP Roadmap for Embedded System on Chip (SoC) Applications

*Cortus announces the expansion of its product range to include a total of four 32-bit embedded microcontroller cores addressing a wider market. The processor family builds on its production proven technology first released with the APS3 ultra low power core.*

**Montpellier, France 21<sup>st</sup> February, 2012.** Cortus S.A., a technology leader in ultra low power, silicon efficient 32-bit processor IP, announces its plan to launch three new microcontroller IP cores as part of its processor roadmap. The new cores share common technology with the highly efficient APS3 core but address complementary market segments. The three new cores will be released over the coming six months.

With the use of sensor, control systems and connectivity technology becoming ubiquitous it is essential that integrated circuits for embedded applications combine adequate processing power, low energy usage and minimal silicon area. The Cortus APS3 has, since entering volume production in 2008, delivered industry-leading performance in terms of DMIPS/mW and DMIPS/mm<sup>2</sup>.

Michael Chapman, CEO Cortus, says “Although APS3 has been very successful in low power embedded applications such as SIM cards, Bluetooth LE, smart meters, encryption/decryption and touchscreen controllers, customers have been asking for a wider range of performance and complexity options”. He adds, “by mid 2012, Cortus will be able to supply microcontroller cores for applications ranging from high throughput floating point control systems down to programmable finite state machines as well as everything in between”.

Under the microcontroller core roadmap, the highly efficient APS3 will be complemented by two new integer and one floating point processor cores. The APS5 will support more complex processor sub-systems requiring caches, co-processors and multi-core architectures. The FPS6 single precision floating point microcontroller core will combine high floating point throughput with a small silicon footprint and low power dissipation.

For small microcontroller subsystems the Cortus will provide an entry-level 32-bit solution with the APS1 processor. This core, with a comparable silicon footprint to existing 8-bit cores such as 8051, will deliver greater computational performance and while dissipating much less power than 8-bit cores. APS1, like other Cortus processors, has been designed to be programmed with C or C++ without the need to use assembly code.

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All Cortus cores share a common technology base with a modern RISC architecture and native 32-bit performance. They all can use the fast, low latency APS bus with Cortus peripherals. Cortus supplies a GNU-based APS toolchain and an Eclipse-based IDE which supports the entire product family. Ports of FreeRTOS, OpenRTOS and Micrium  $\mu$ C/OSII are available for the processor product range.

Cortus will be exhibiting from 28<sup>th</sup> February to 1<sup>st</sup> March on stand 5-143 at Embedded World 2012 in Nürnberg, Germany

**About Cortus S.A.**

Cortus S.A. is the cost/performance leader for 32 bit processor IP for embedded systems. Cortus cores are used in applications where one or more of small silicon footprint, low power consumption, good code density/small code memory size and high performance are important.

<http://www.cortus.com>

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